Remarks

Amendments to the title, specification, and claims have been presented.

In the specification, a typographical error has been corrected.

The title has been changed to be more descriptive of the subject matter of the claimed invention.

Various amendments to claims 1, 3, 12, 17, 20, 23, and 24 have been presented to clarify and/or provide antecedent basis in response to 112 rejections. These amendments were not done for the purpose of overcoming cited art.

Various amendments to claims 1, 9, 17, 20, 23, and 24 have been presented to change "based upon" to "based at least in part upon." This proposed change is consistent with other claims and the specification, and is intended to remove an element that may have the potential to be unnecessarily restrictive. These amendments were not done for the purpose of overcoming cited art.

Various amendments to claims 1, 9, 17, and 20 have been presented to clarify that selection is between data signals. These amendments were not done for the purpose of overcoming cited art.

No new matter has been added as a result of these amendments and support for the changes is found throughout the original specification.

Claim Rejections

35 USC 112, second paragraph rejection of claims 1-8 and 17-27

In the Office Action claims 1-8 and 17-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claims the inventive subject matter. The Applicant presents the above amendments to more particularly point out and distinctly claim the inventive subject matter. Therefore the Applicant respectfully requests that the Examiner withdraw these rejections of these claims.

35 U.S.C. 102(e) rejection of claims 12 and 20 over Migita

In the Office Action claims 12 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Migita. The Applicant respectfully traverses these rejections of these claims.

Claim 12, for example, recites:

> 12. A method of passing data between a first time domain and a second asynchronous time domain, the method comprising:
> receiving a first data signal generated with respect to a first clock signal associated with said first time domain;
> receiving a second data signal representing said first data signal delayed by a first measure such that during transition of said first data signal said second data signal is valid, and during transition of said second data signal said first data signal is valid; and
> selecting between said first and second data signals based at least in part upon the state of a second clock signal associated with said second time domain.

The Examiner states that the selecting between the first and second data signals is found in Migita at col. 5, lines 13-20 and at col. 6, lines 24-30, 39-42. The Applicant respectfully traverses this statement.

Migita does not teach, either expressly or inherently, choosing between a first and second data signal, where the first data signal is generated with respect to a first clock signal and the second data signal is the first data signal delayed by a first measure.

Briefly, Migita teaches inputting data signals (D11-D12), generated with respect to a first time domain, into a latch circuit. The latch circuit will then simultaneously output latch data (L11-L14) representative of the input data (D11-D12) sampled at CK2. The latch data (L11-L14) is not the same as the input data (D11-D12). Migita further teaches a process to determine which of the latch data (L11-L12) will be output as synchronous data based on comparison data (C11-C13). Therefore, the selection taught by Migita is between latch data, not input data. Nowhere in Migita is it suggested, discussed, or described that selection between any of the input data (D11-D14) is to be done based at least in part upon the second clock signal.

The Applicant submits that because all of the elements of claim 12, for example, are not described, either expressly or inherently, an anticipation rejection is improper. It is therefore respectfully requested that the Examiner withdraw this rejection of this claim.

The Applicant also traverses the rejection of claim 20 based on Migita.

Amended claim 20, for example, recites:

> 20. An integrated circuit comprising:
> a first delay circuit to generate a selector signal based at least in part upon an input reference signal of a first time domain;
> a second delay circuit to generate a delayed data signal based at least in part upon an input data signal; and
> selection logic coupled to the first and second delay circuits to select between said input data signal and said delayed data signal based at least in part upon a state of the selector signal in accordance with an input clock signal of a second time domain, such that at any given sampling point of the input clock signal, the selector signal indicates valid data.

The Examiner briefly states that this claim is the system that is designed to carry out the method steps, presumably of claim 12, and therefore Migita teaches the claimed system in Figures 1 and 5. However, the elements of claim 20 do not mirror the elements of claim 12, and therefore any rationale applied to the rejection of claim 12 does not necessarily transfer to examination of claim 20.

It is unclear to the Applicant, which of the embodiments of Migita, Figure 1 or Figure 5, the Examiner believes anticipate claim 20. However, after reviewing both embodiments, it is clear that neither of these embodiments describes, either expressly or inherently, all of the elements of claim 20.

The embodiment depicted by Figure 1 does not describe, either expressly or inherently, "a <u>first delay circuit to generate a selector signal</u> based at least in part upon an input reference signal of a first time domain" as required by claim 20. In Figure 1, the delay circuits **31**, **32**, and **33** generate delayed data packets **D12-D14**, respectively. These data packets are not the same as the selector signal element discussed in claim 20. The selector signal is of the type that is used by the selection logic for selecting

between the input data signal and the delayed data signal, it is not the data signals themselves.

The embodiment depicted by Figure 5 does not describe, either expressly or inherently, the "first delay circuit to generate a selector signal based at least in part upon an input reference signal of a first time domain" as required by claim 20. CK3 of Figure 5, which is input into the delay section **3A**, is a reference clock of the clock CK2 of the second time domain, not the first time domain. See column 7, line 32.

Even assuming that the selector signal was based at least in part upon a reference signal of the first time domain, which the Applicant disputes, this embodiment still does not describe, either expressly or inherently, "a second delay circuit to generate a delayed data signal based upon an input data signal" as required by claim 20. The discussion of Figure 5, explicitly states that, unlike the first embodiment, the Figure 5 embodiment comprises a delay section for delaying the clock CK3 instead of delaying the data **D11**. See column 7, line 31.

Thus, Applicant submits that because all of the elements of claim 20 are not described, either expressly or inherently, an anticipation rejection is improper. It is therefore respectfully requested that the Examiner withdraw this rejection of this claim.

Allowable Subject Matter

Claims 9-11 are allowed over prior art. Claims 13-19 and 21-27 were objected to but would be allowable if rewritten as independent claims, as appropriate. The Applicant requests that the Examiner withdraw these objections to claims 13-19 and 21-27 due to the reasons discussed above with respect to the patentability of the underlying base claims 12 and 20, respectively.

Conclusion and Epilogue

In view of the foregoing, the Applicant respectfully submits that claims 1-27 as presented are in condition for allowance. Thus, early issuance of Notice of Allowance is respectfully requested.

If the Examiner has any questions, he is invited to contact the undersigned at (503) 796-2972.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393. A Fee Transmittal is enclosed in duplicate for fee processing purposes.

Respectfully submitted,
SCHWABE, WILLIAMSON & WYATT, P.C.

Dated: 10/26/04

Nathan R. Maki
Registration No. 51,110

Pacwest Center, Suites 1600-1900
1211 SW Fifth Avenue
Portland, Oregon 97204
Telephone: 503-222-9981